REMARKS

I. General

Claims 1-23 are pending in the present application. Claims 1-2, 13-18, and 20-21 stand rejected under 35 U.S.C. § 102. Claims 3-9, 11, 12, 19, 22, and 23 stand rejected under 35 U.S.C. § 103. Claims 1-23 stand rejected under 35 U.S.C. § 112. Claims 2, 14-19, and 22 stand objected to because of informalities. The drawings stand objected to. Applicant respectfully traverses the rejections and objections of record.

Applicant has noted the Examiner's comments regarding the Information Disclosure Statement filed February 11, 2001. However, Applicant is unable to determine the reason for the Examiner having not considered references G, H, and I included therein. From the introductory statements it appears that perhaps the Examiner received illegible copies of these references. Applicant's file copies of these references are of good quality and, therefore, it is believed that the xerographic copies submitted in the Information Disclosure Statement were legible. However, Applicant is again submitting copies of these references in an Information Disclosure Statement being filed with the present Amendment in case the Examiner's copies previously submitted were illegible. If the copies of the references provided herewith are not acceptable to the Examiner, Applicant respectfully requests that the Examiner provide detail with respect to the nature of the problem with the references.

The Examiner points out that the various parts of reference F were published at different dates. Accordingly, Applicant submits herewith an Information Disclosure Statement in which these parts have been separately identified as requested by the Examiner.

Figures 6, 7, and 8 have been amended to correct informalities discovered during the preparation of the present Amendment. In particular, lines connecting summers 615 and 620 of Figures 6, 7, and 8, summers 735 and 730 of Figures 7 and 8, summers 845 and 840 of Figure 8 included incorrect arrow heads in the formal drawings filed April 16, 2002. These figures have been corrected to correspond with the description provided at page 17, lines 17-25, page 18, lines 5-14, and page 18, line 26, through page 19, line 7. No new matter has been added.

II. The Drawing Objections

Figure 5 stands objected to as not including reference sign "5" as mentioned in the specification. Applicant submits herewith a proposed drawing amendment adding the reference sign to Figure 5.

Figure 8 stands objected to as not including the reference sign "842" as mentioned in the specification. Applicant submits herewith a proposed drawing amendment adding the reference sign to the figure.

Figure 9 stands objected to as requiring the legend "Prior Art." Applicant submits herewith a proposed drawing amendment adding the legend to the figure.

Figure 12 stands objected to as not including the reference signs "1204" and "1205" as mentioned in the specification. Applicant submits herewith a proposed drawing amendment adding the reference signs to Figure 12.

Figure 12 further stands objected to because an arrow flow is not labeled between elements 122 and 1023. Applicant is unable to find element 1023 in Figure 12 and, therefore, presumes that the Examiner intended to state element 1203. However, proceeding under this assumption Applicant is unable to identify any arrow flow which is properly objectionable due to omission of a label. Applicant notes that many unlabeled arrow flows extend from element 122 and can find no authority for requiring addition of a label to any such arrow flow. Accordingly, it is believed that the objection to Figure 12 is improper and should be withdrawn. If, however, the Examiner maintains the objection to Figure 12 in light of the above, Applicant respectfully solicits the Examiner to provide detail with respect to the basis for requiring labeling the arrow flow and a suggestion as to how the arrow flow is expected to be labeled.

✓ ok

Figure 12 stands objected to as including the reference sign "120" which is not mentioned in the specification. Applicant's review of Figure 12 does not reveal reference sign "120" and, therefore, Applicant presumes that the Examiner intended reference sign "1200." The specification mentions reference sign "1200" of Figure 12 at page 25, line 29. Accordingly, Applicant requests that the objection to Figure 12 be withdrawn.

✓ ok

The figures stand objected to generally as not including the reference signs "210," "211," "MASH A," and "MASH B" mentioned on page 21, lines 21-23, of the specification. However, these words as appearing in the specification at page 21, lines 21-23, are not reference signs. In particular, "210" and "211" are the reference signals (described throughout the specification as varying in the least significant bit between a first modulator stage and subsequent modulator stages) provided to the quantizers of two modulator configurations, identified as "MASH A" and "MASH B." As there is no reference to the figures intended, the objection to the figures is improper and should be withdrawn.

ok

III. The Claim Objections

Claims 2, 14-19, and 22 stand objected to because of informalities asserted to be present therein by the Examiner. For example, with respect to claim 2, the Examiner suggests that the phrase "an output of said set of differentiators" recited therein should read "an output of each of said set of differentiators" for accuracy. Applicant has amended claim 2 as suggested by the Examiner. The foregoing amendment is believed to address the basis of the objection to claim 14, dependent from claim 2.

In objecting to claim 15, the Examiner asserts that the phrase "an input" should be "an input signal." Applicant has amended claim 15 as suggested by the Examiner.

With respect to claim 16 the Examiner suggests that the phrase "reversed input" should be "inversed input signal." However, the claim recites a "revised input," not a "reversed input." As recited in the claim, a revised input is formed by subtracting the quantized signal from the input signal. Accordingly, Applicant asserts that the claim language is accurate and proper. Applicant respectfully requests that the objection to claim 16 based upon recitation of the phrase "revised input" be withdrawn.

not agree

Also with respect to claim 16, the Examiner suggests that the phrase "said quantized signal" should be "quantized signal as said first modulated signal." Applicant has amended the claim in this regard as suggested by the Examiner.

In objecting to claim 17, the Examiner suggest that "signal" and "said subsequent modulated signal" should be "signals" and "a subsequent modulated signal," respectively.

Applicant has amended the claim as suggested by the Examiner. The foregoing amendment is believed to address the basis of the objection to claim 18, dependent from claim 17.

With respect to claim 19 the Examiner suggests that the phrase "said producing said first intermediate modulating signal step" should be "said step of producing said first intermediate modulating signal." Applicant has amended the claim as suggested by the Examiner.

In objecting to claim 22, the Examiner suggest that the phrase "said producing said first intermediate modulating signal step" should be "said means for producing said first intermediate modulating signal." Applicant has amended the claim as suggested by the Examiner.

The foregoing redress the objections of record with respect to claims 2, 14-19, and 22. Moreover, the amendments discussed above, made in response to the claim objections, do not present new matter and have not narrowed the scope of the claims.

IV. The 35 U.S.C. § 112 Rejections

A. The Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 1-23 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner asserts that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention.

In rejecting claim 1, the Examiner asserts that the claim recites a set of differentiators disposed in each of said at least one subsequent stage but that Figure 8 shows a second stage which includes one differentiator only. It appears that the source of the Examiner's consternation is recital of "a set of differentiators" when only one differentiator is shown with respect to a second stage. However, a set, in the ordinary and customary use of that term, can include a single element. As such, the language of claim 1 is fully enabled by the specification.

The Examiner asserts that recitation of the first delta-sigma modulator comprising a multi-stage delta-sigma modulator in claim 10 is unsupported by the specification because

Figure 8 shows a first delta-sigma modulator comprising a one-stage delta-sigma modulator only. However, the disclosure of Figure 8 is not restricted to the Examiner's characterization of that figure. Figure 6 clearly shows a multi-stage delta-sigma modulator. Additionally, Figure 7 shows a multi-stage delta-sigma modulator wherein a delta-sigma modulator stage has been added to the delta-sigma modulator of Figure 6. Similarly, Figure 8 shows a multi-stage delta-sigma modulator wherein a delta-sigma modulator stage has been added to the delta-sigma modulator of Figure 7. Accordingly, it is clear from these figures that the first two stages of the multi-stage delta-sigma modulator of Figure 8 are themselves are a multi-stage delta-sigma modulator and, likewise, the first three stages of the multi-stage delta-sigma modulator of Figure 8 are themselves a multi-stage delta sigma modulator. Accordingly, it is clear from the figures that a characterization Figure 8 is that a first stage thereof comprises a multi-stage delta-sigma modulator. As such, Applicant respectfully asserts that the claim is fully enabled by the disclosure. Moreover, as claim 10 is not rejected over the art of record, Applicant asserts that claim 10 should stand allowed.

disagree

With respect to claim 15, the Examiner asserts that no circuitry is shown for programming reference signals as recited therein. However, claim 15 recites a method including a programming step and, therefore, a drawing of circuitry is not believed to be necessary to enable the claim. Drawings are generally not required for enablement of a method, see M.P.E.P. § 608.02. Moreover, the specification describes programming reference signals according to embodiments to be different by one least significant bit, giving as an examples a first reference signal of 210 and a second reference signal of 211, see page 17, lines 24-24, and page 21, lines 20-22. It is respectfully asserted that one of ordinary skill in the art would be enabled to program a reference signal as set forth above without reference to any circuitry and without undue experimentation. Accordingly, Applicant respectfully asserts that claim 15 is enabled as required under 35 U.S.C. § 112, first paragraph, by the accompanying specification.

In rejecting claim 20 under 35 U.S.C. § 112, first paragraph, the Office Action states that claim 20 recites means for providing the modulated output signal to an output of the multi-order delta-sigma modulator but no additional circuitry is shown other than the summing circuit 600 of Figure 8 for providing the modulated output signal to an output of the multi-order delta-sigma modulator. However, Figure 8 clearly shows output 6001 coupled to summing circuit 600 via a transmission line for providing the modulated output signal to an

disagree

output of the multi-order delta-sigma modulator. Applicant respectfully asserts that the claim is fully enabled by this disclosure.

B. The Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 4, 13, and 14 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Examiner asserts that claim 4 is unclear with respect to the number of digital differentiators to be used in the set of differentiators in each of the subsequent stages. Although not conceding that the claim as originally presented is unclear, Applicant has amended claim 4 to delete recitation of "substantially" in an effort to present a claim which the Examiner will find acceptable.

The Examiner identifies recitation of the invention being constructed substantially on a single integrated circuit substrate as the basis for the 35 U.S.C. § 112, second paragraph, rejections of claims 13 and 14. Applicant has amended the preamble of claim 13 substantially as suggested by the Examiner so as to recite "the modulator of claim 1" rather than "the invention of claim 1." However, Applicant has not cancelled claim 14 as suggested by the Examiner because that claim recites an additional component included on the integrated circuit substrate. Claim 14 has, however, been amended similar to claim 13 to change the preambular recitation of "invention" and insert therefor "modulator."

It is believed that the foregoing redress the 35 U.S.C. § 112, second paragraph, rejections of record. Accordingly, it is believed that the claims are allowable over 35 U.S.C. § 112.

V. The 35 U.S.C. § 102 Rejections

Claims 1, 2, 13-18, 20, and 21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Adachi et al., patent number 6,717,998 (hereinafter *Adachi*). Applicant respectfully traverses the 35 U.S.C. § 102 rejections of record.

Applicant submits the Declaration of Jerry Thomas Bolton, Jr. Submitted Under 37 C.F.R. § 1.131 presenting evidence that the invention of claims 1-11, 13-18, 20, 21, and 23 was actually reduced to practice before December 12, 2000. The earliest date available with

respect to *Adachi* for the 35 U.S.C. § 102(e) rejection is December 12, 2000. Accordingly, *Adachi* is not available as prior art with respect to at least claims 1-11, 13-18, 20, 21, and 23.

Moreover, to anticipate a claim under 35 U.S.C. § 102, a reference must teach every element of the claim, see M.P.E.P. § 2131. Additionally, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim," see M.P.E.P. § 2131, citing Richardson v. Suzuki Motor Co., 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989).

Independent claim 1 recites "each of said at least one subsequent delta-sigma modulators having a reference signal variable in relation to said first reference signal . . . ." Similarly, independent claim 15 recites "programming at least one of said subsequent references to be different from said first reference." Claim 20 recites "selected of said subsequent reference signals are selectively variable in relation to said first reference signal . . . ." In rejecting the claims, the Office Action states that the first delta-sigma stage of *Adachi* has a first reference signal Q1 and the second delta-sigma stage of *Adachi* has a second reference signal Q2, relying on column 22, lines 24-28, see the Office Action at page 7. However, Applicant can find no disclosure in the identified portion of *Adachi*, nor through Applicant's review of *Adachi*, which teaches that Q2 is different or variable with respect to Q1. Indeed, the subsequent discussion in *Adachi* appears to reference these signals simply as Q, indicating that there is no difference intended, see column 23, lines 5-9.

In light of the foregoing, Applicant respectfully asserts that *Adachi* does not show the identical invention in as complete detail as is contained in the claim. Therefore, claims 1, 15, and 20, and the claims dependent therefrom, are patentable over the 35 U.S.C. § 102 rejections of record.

Moreover, the dependent claims add additional limitations not present in the applied reference. For example, claims 13 and 14 recite the modulator being constructed substantially on a single integrated circuit substrate. *Adachi* does not provide any disclosure with respect to the modulators therein being constructed on an integrated circuit substrate.

Claim 16 recites, with respect to producing the first modulated signal, subtracting the quantized signal from the input signal to form a revised input. *Adachi* does not teach this

aspect of the claims, see e.g., adder 208 and output of quantizer 202. Claim 17 recites, with respect to producing subsequent modulated signals, subtracting the subsequent modulated signal from a prior stage error signal to produce a modified quantized error signal. *Adachi* does not teach this aspect of the claims, see e.g., adder 228 and adder 210. Similarly, claim 18 recites, with respect to producing the subsequent modulated signal of each subsequent modulated signals, subtracting the subsequent modulated signal from the integrated error signal to form a subsequent stage error signal. *Adachi* does not teach this aspect of the claims, see e.g., adder 228.

VI. The 35 U.S.C. § 103 Rejections

Claims 3, 12, 19, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Adachi* in view of Duffy et al., patent number 5,196,850 (hereinafter *Duffy*). Claims 5-9, 11, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Adachi* in view of the prior art of Figure 5 of the present application. Claim 4 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Adachi* in view of *Duffy* in further view of the prior art of Figure 5 of the present application. Applicant respectfully traverses the 35 U.S.C. § 103 rejections of record.

To establish a *prima facie* case of obviousness, three basic criteria must be met, see M.P.E.P. § 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Without conceding the second criteria, Applicant respectfully asserts that the references lack proper motivation to combine in addition to lacking all the claim limitations.

In the 35 U.S.C. § 103 rejection of claims 3, 12, 19, and 22, the Office Action states that it would have been obvious to one of ordinary skill in the art to use a digital signal as taught by *Duffy* in the circuit of *Adachi* when the circuit of *Adachi* is operated in digital conversion, see the Office Action at page 9. The language of the recited motivation is circular in nature, stating that it is obvious to make the modification because it is obvious to achieve the result. Such language is merely a statement that the reference can be modified,

and does not state any desirability for making the modification. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination, M.P.E.P. § 2143.01, citing In re Mills, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). Thus, the motivation provided by the Examiner is improper, as the motivation must establish the desirability for making the modification.

In rejecting claims 5-9, 11, and 23, the Office Action states that it is well known in the delta-sigma modulator art that higher order delta-sigma modulators are commonly used, as shown in the prior art of Figure 5 of the present application. Therefore, the Office Action concludes that it would have been obvious to have included delta-sigma modulator stages in addition to the two stages shown in *Adachi*. However, *Adachi* expressly teaches the stages thereof are each second order delta-sigma modulator stages, see e.g., column 9, lines 52-55, and column 21, lines 25-27. *Adachi* further teaches that the two second order delta-sigma modulator stages thereof provide a forth order delta-sigma modulator, see column 22, lines 65-67. There is nothing to have suggested to one of ordinary skill in the art to provide additional stages in the delta-sigma modulator of *Adachi* in order to go beyond a forth order implementation in the forth order delta-sigma modulator disclosure of Figure 5 of the present application. Accordingly, it is respectfully asserted that proper motivation to modify the delta-sigma modulator of *Adachi* as proffered by the Examiner has not been provided.

With respect to claims 6-9 and 23, the Examiner concedes that *Adachi* does not disclose differences in the reference signals as specifically recited in these claims. However, the Examiner opines that such specific differences are a design choice. The Examiner is asserting it is obvious to try all possible combinations of differences between reference signals in order to achieve the specific embodiments recited in Applicant's claims as presented. However, application of an obvious to try rational in support of an obviousness rejection under 35 U.S.C. § 103 is improper, see M.P.E.P. § 2145(X)(B).

Claim 4 stands rejected as being unpatentable over *Adachi* in view of *Duffy* as applied to claim 3 and further in view of the prior art of Figure 5 of the present application. In particular, the Office Action states that it would have been obvious to include more states in *Adachi* to reduce the correlation between the input and the quantization noise. However, claim 4 recites the set of differentiators comprises a number of digital differentiators equal to a number of the modulator stages before the subsequent stage on which the set of

differentiators is disposed. This aspect of the claims remains wholly unaddressed by the rejection of record. Accordingly, claim 4 is allowable over the rejections of record.

VII. Summary

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 06-2380, under Order No. 49581/P023US/09906909 from which the undersigned is authorized to draw.

Dated: July 21, 2004

Respectfully submitted,

By _____

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Attachments

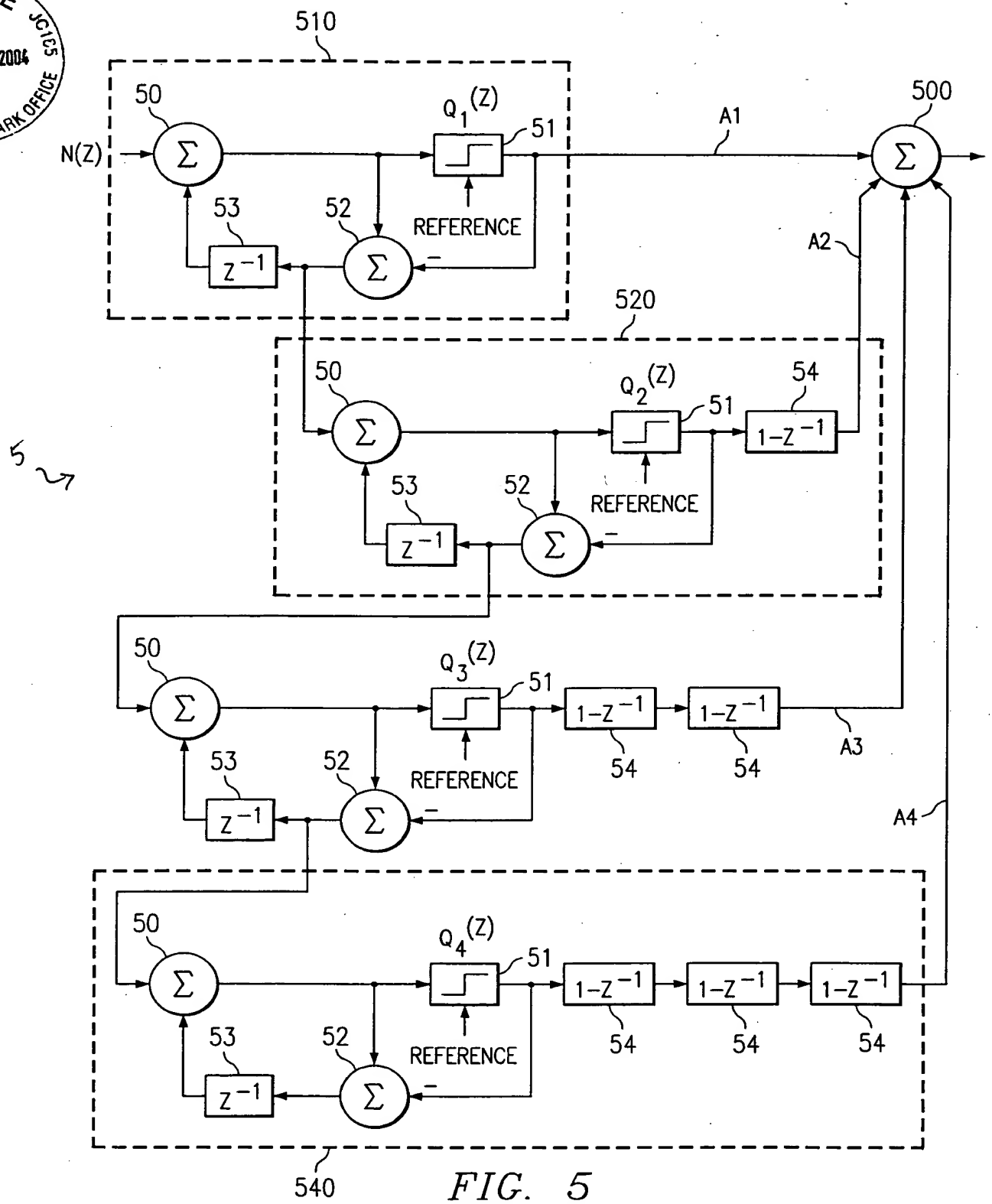


FIG. 5
(PRIOR ART)

FIG. 6

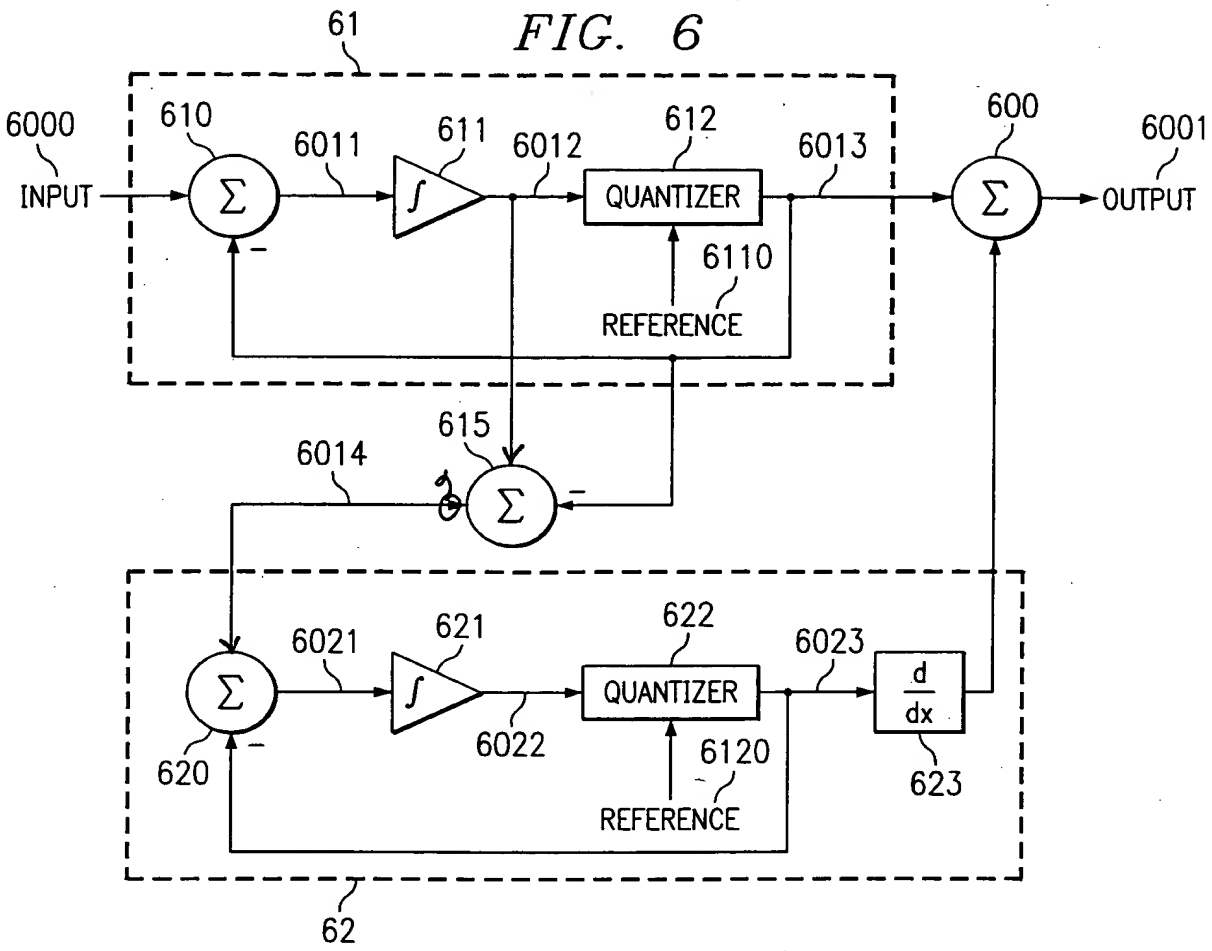
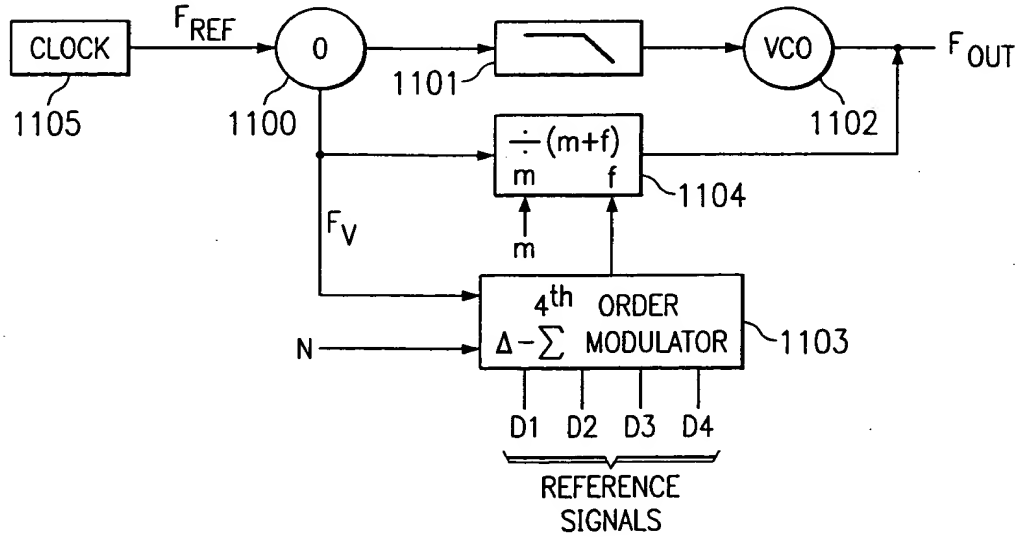


FIG. 11



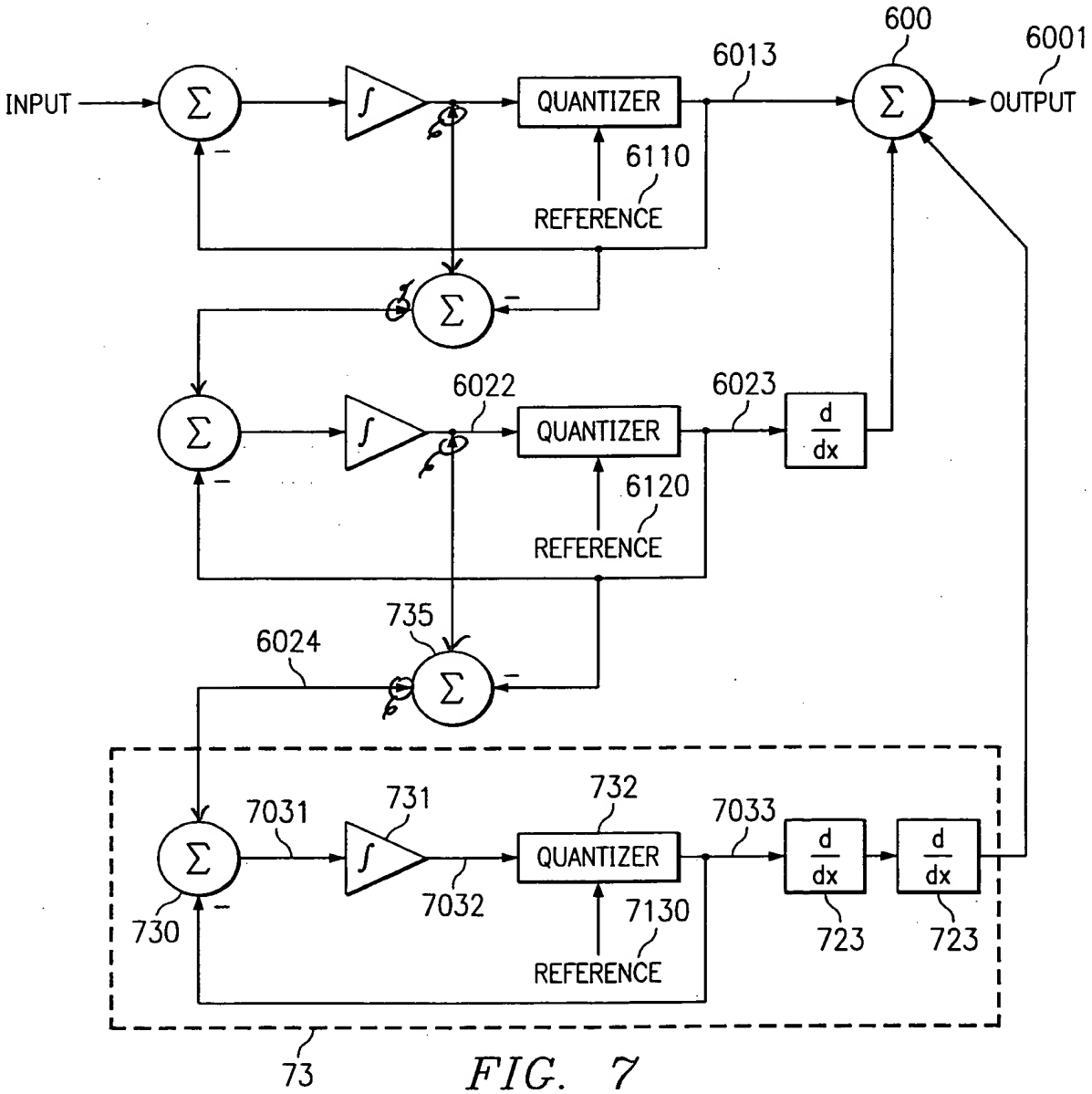


FIG. 7

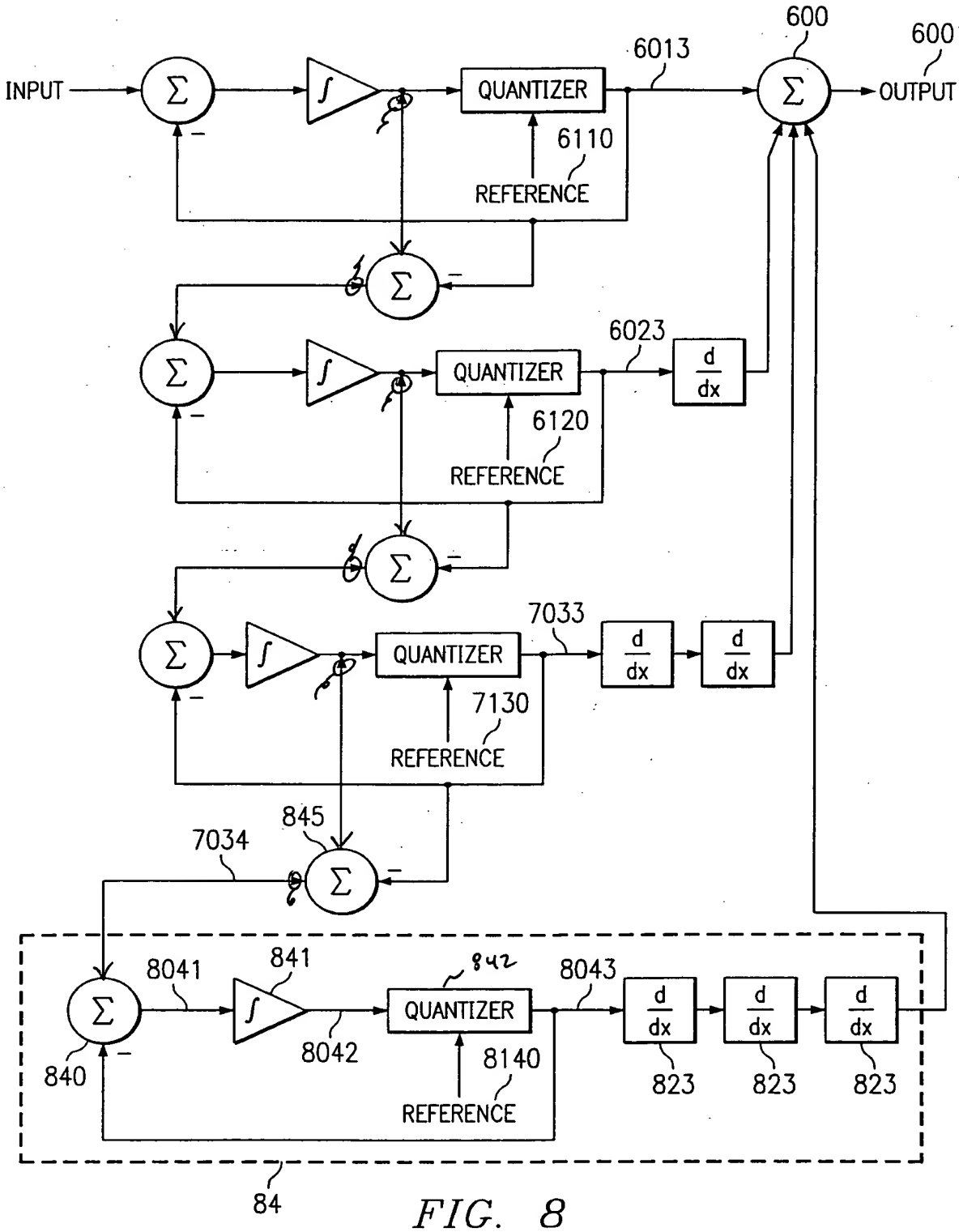


FIG. 8

FIG. 9 (Prior Art)

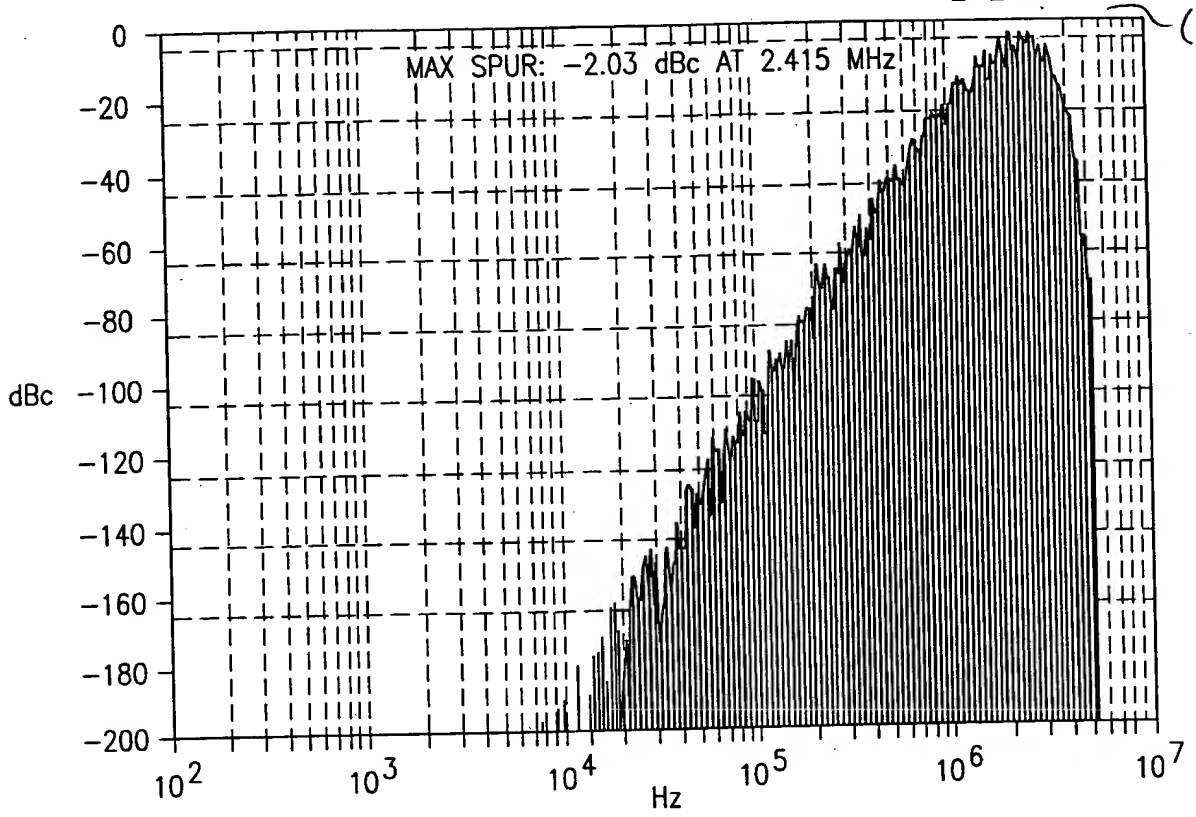
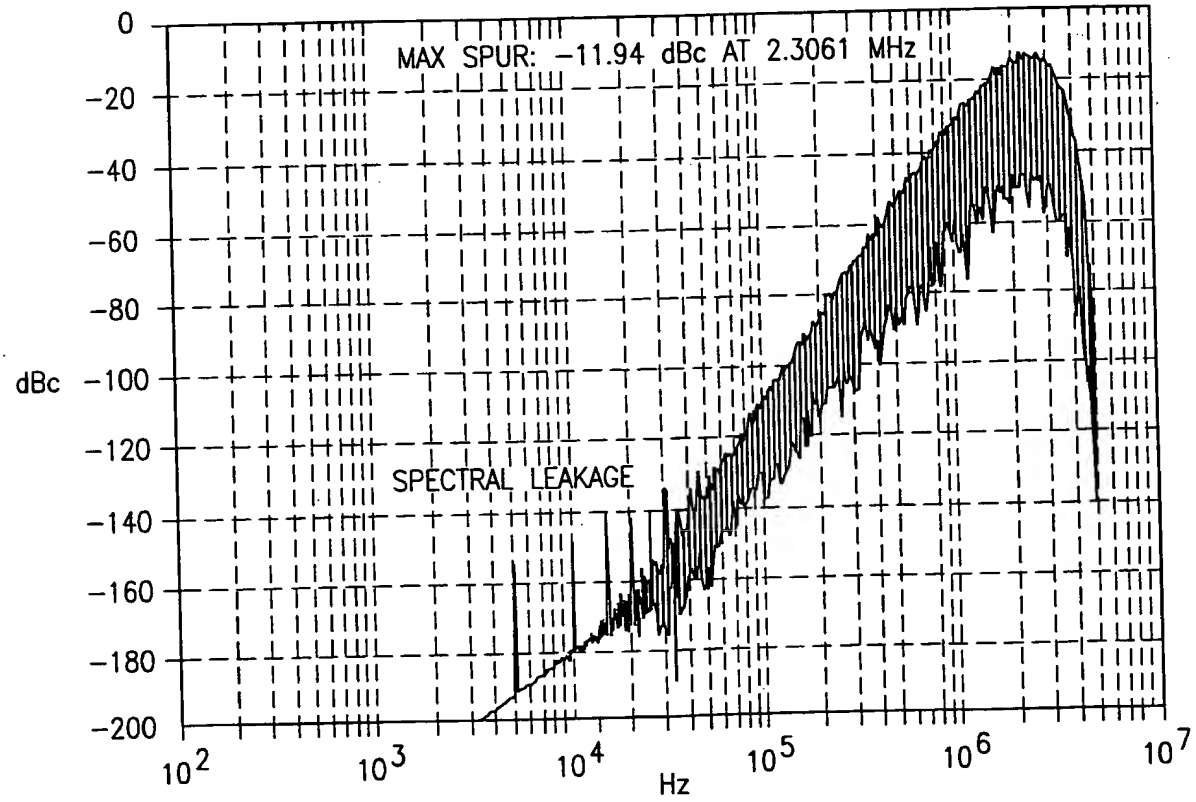


FIG. 10



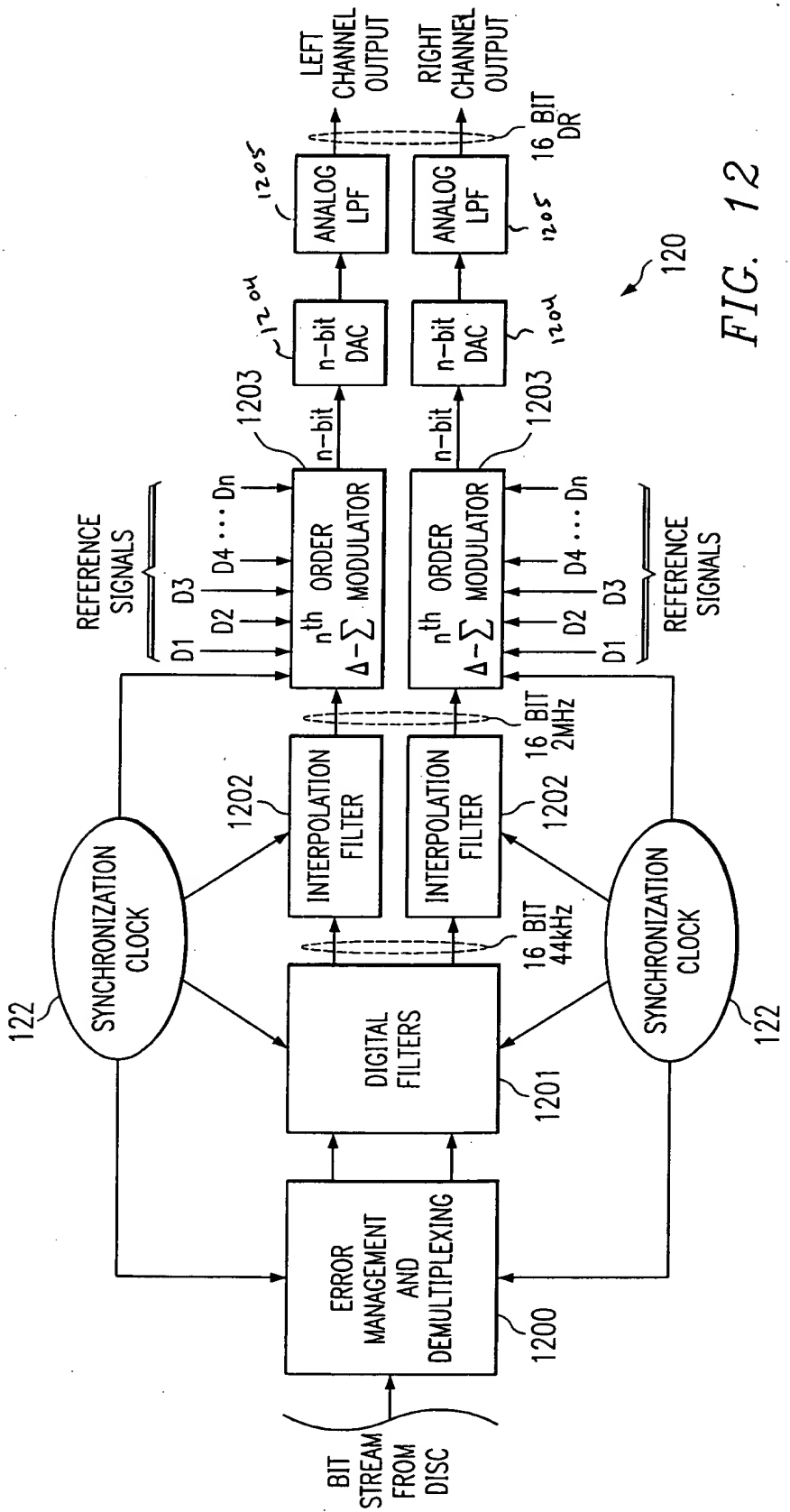


FIG. 12